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ABSTRACT

An apparatus and methods for modifying isolation structure configurations for MOS devices to either induce or reduce tensile and/or compressive stresses on an active area of the MOS devices. The isolation structure configurations according to the present invention include the use of low-modulus and high-modulus, dielectric materials, as well as, tensile stress-inducing and compressive stress-inducing, dielectric materials, and further includes altering the depth of the isolation structure and methods for modifying isolation structure configurations, such as trench depth and isolation materials used, to modify (i.e., to either induce or reduce) tensile and/or compressive stresses on an active area of a semiconductor device.